WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a plurality of word lines, a plurality of bit lines and a plurality of memory cells, said plurality of memory cells each being connected to one of said plurality of word lines and one of said plurality of bit lines;

a Y decoder configured to drive said plurality of bit lines; and

a disconnecting device provided between at least one of said plurality of bit lines and said Y decoder, and being configured to electrically disconnect said at least one of said plurality of bit lines and said Y decoder.

2. The semiconductor memory according to claim 1, wherein

said disconnecting device includes a plurality of disconnecting devices, capable of electrically disconnecting those of said plurality of bit lines on which said plurality of disconnecting devices are provided integrally from said Y decoder.

3. The semiconductor memory according to claim 1, wherein

said disconnecting device includes a plurality of disconnecting devices, capable of electrically disconnecting those of said plurality of bit lines on which said plurality of disconnecting devices are provided individually from said Y decoder.

4. A semiconductor memory comprising:

a plurality of memory cells, each being connected to one of a plurality of word lines and one of a plurality of bit lines;

a Y decoder configured to drive said plurality of bit lines; and

a charge pump circuit and a port circuit, each being connected to said Y decoder through a switching circuit.